

## ABSTRACT

A semiconductor apparatus comprises a processor having  
an instruction register inside thereof, a pseudorandom number  
5 generating device activated in response to a test operation  
and generating pseudorandom numbers, an input switchover device  
for switching over between data input in normal operation and  
input of the pseudorandom numbers from the pseudorandom number  
generating device in the test operation to thereby output the  
10 data or pseudorandom numbers to the instruction register. The  
pseudorandom numbers generated in the pseudorandom number  
generating device are inputted to the instruction register  
via the input switchover device so that the random instructions  
are implemented and a random test is implemented with an  
15 activation rate equivalent to the same in the normal operation.

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